**Differences**

| **VON NEUMAN ARCHITECTURE** | **HARVARD ARCHITECTURE** |
| --- | --- |
| It is ancient computer architecture based on stored program computer concept. | It is modern computer architecture based on Harvard Mark I relay based model. |
| Same physical memory address is used for instructions and data. | Separate physical memory address is used for instructions and data. |
| There is common bus for data and instruction transfer. | Separate buses are used for transferring data and instruction. |
| Two clock cycles are required to execute single instruction. | An instruction is executed in a single cycle. |
| It is cheaper in cost. | It is costly than Von Neumann Architecture. |
| CPU can not access instructions and read/write at the same time. | CPU can access instructions and read/write at the same time. |
| It is used in personal computers and small computers. | It is used in micro controllers and signal processing. |

CISC:

A **complex instruction set computer** (**CISC**) is a [computer architecture](https://en.wikipedia.org/wiki/Computer_architecture) in which single [instructions](https://en.wikipedia.org/wiki/Instruction_set_architecture) can execute several low-level operations (such as a load from [memory](https://en.wikipedia.org/wiki/Memory_(computers)), an [arithmetic](https://en.wikipedia.org/wiki/Arithmetic) [operation](https://en.wikipedia.org/wiki/Operator_(programming)), and a [memory store](https://en.wikipedia.org/wiki/Memory_(computers))) or are capable of multi-step operations or [addressing modes](https://en.wikipedia.org/wiki/Addressing_mode) within single instructions.

Examples of CISC architectures include complex [mainframe computers](https://en.wikipedia.org/wiki/Mainframe_computer) to simplistic microcontrollers where memory load and store operations are not separated from arithmetic instructions. Specific instruction set architectures that have been retroactively labeled CISC are [System/360](https://en.wikipedia.org/wiki/System/360) through [z/Architecture](https://en.wikipedia.org/wiki/Z/Architecture), the [PDP-11](https://en.wikipedia.org/wiki/PDP-11) and [VAX](https://en.wikipedia.org/wiki/VAX) architectures, and many others. Well known microprocessors and microcontrollers that have also been labeled CISC in many academic publications include the [Motorola 6800](https://en.wikipedia.org/wiki/Motorola_6800), [6809](https://en.wikipedia.org/wiki/6809) and [68000](https://en.wikipedia.org/wiki/68000)-families; the Intel [8080](https://en.wikipedia.org/wiki/8080), [iAPX432](https://en.wikipedia.org/wiki/IAPX432) and [x86](https://en.wikipedia.org/wiki/X86)-family; the Zilog [Z80](https://en.wikipedia.org/wiki/Z80), [Z8](https://en.wikipedia.org/wiki/Zilog_Z8) and [Z8000](https://en.wikipedia.org/wiki/Z8000)-families; the [National Semiconductor](https://en.wikipedia.org/wiki/National_Semiconductor) [32016](https://en.wikipedia.org/wiki/32016) and [NS320xx](https://en.wikipedia.org/wiki/NS320xx)-line; the MOS Technology [6502](https://en.wikipedia.org/wiki/6502)-family; the Intel [8051](https://en.wikipedia.org/wiki/8051)-family; and others.

What Is RISC?

A Reduced Instruction Set Computer is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions rather than the highly-specialized set of instructions typically found in other architectures. RISC is an alternative to the Complex Instruction Set Computing (CISC) architecture and is often considered the most efficient CPU architecture technology available today.

With RISC, a central processing unit (CPU) implements the processor design principle of simplified instructions that can do less but can execute more rapidly. The result is improved performance. A key RISC feature is that it allows developers to increase the register set and increase internal parallelism by increasing the number of parallel threads executed by the CPU and increasing the speed of the CPU's executing instructions. ARM, or “Advanced RISC Machine” is a specific family of instruction set architecture that’s based on reduced instruction set architecture developed by Arm Ltd. Processors based on this architecture are common in smartphones, tablets, laptops, gaming consoles and desktops, as well as a growing number of other intelligent devices.

